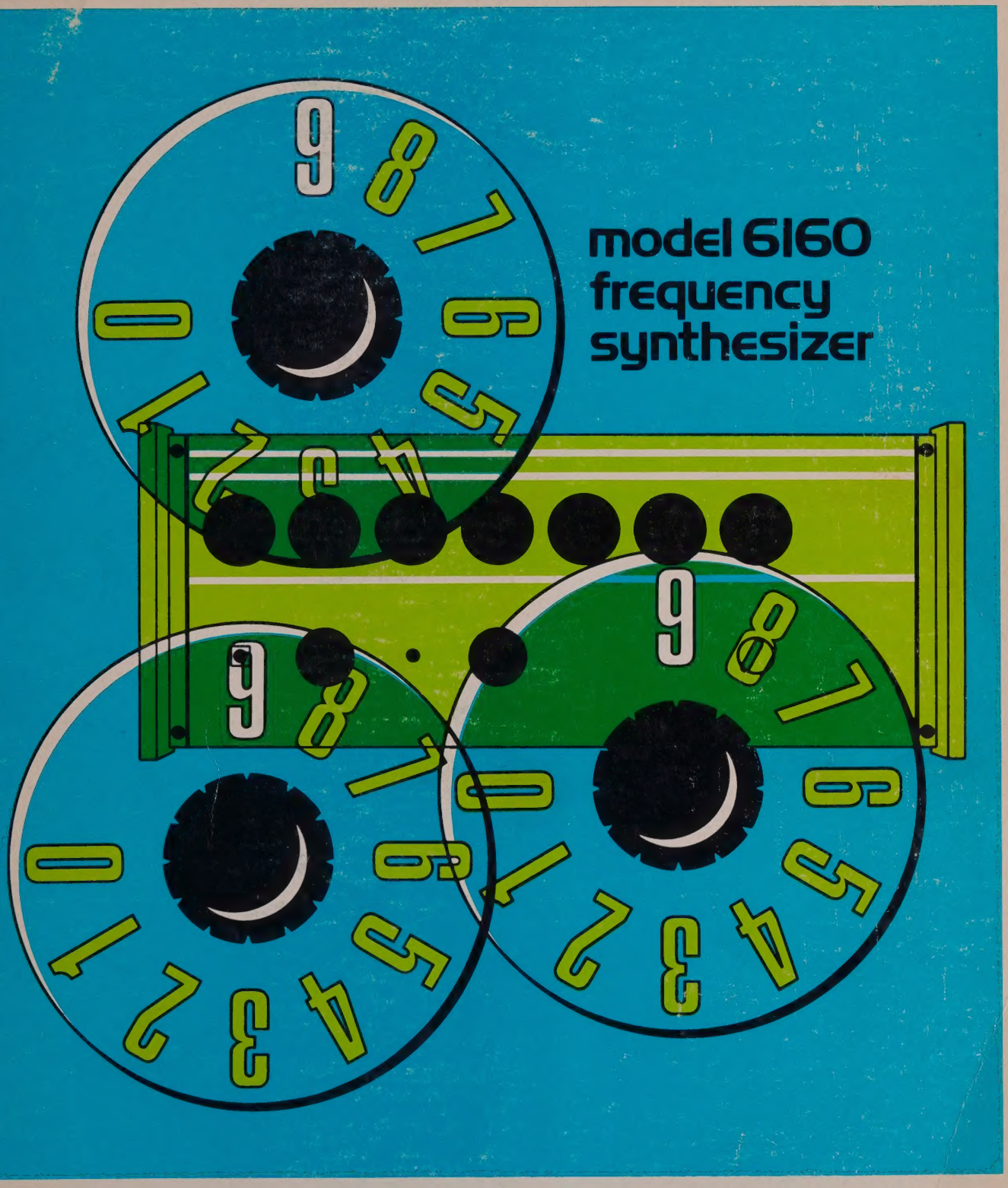
model 6160 frequency synthesizer



student handout

FLUKE®

Forward

This training course has been prepared by the Customer Service Department of the John Fluke Mfg. Co., Inc. to assist the experienced technician to understand how the instrument works, how to calibrate it and how to maintain it. Should you have any questions, comments or suggestions about this course of instruction, please feel free to communicate them to the Training Department by letter or telephone.

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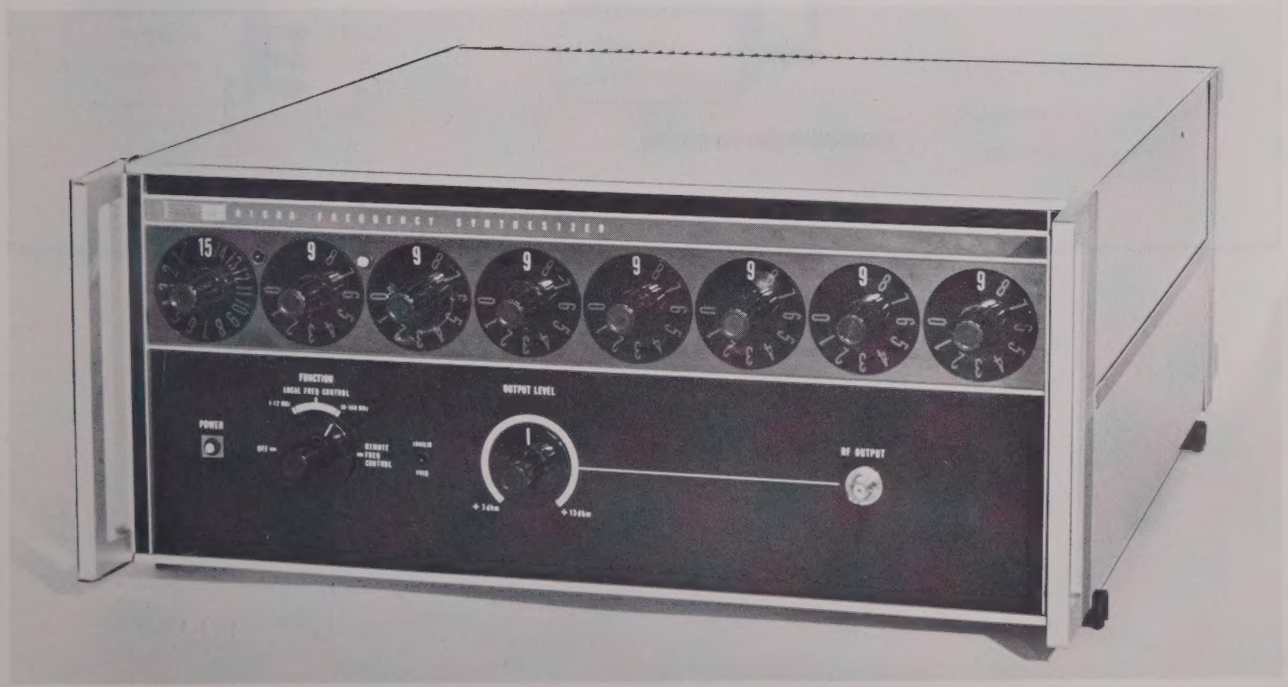


INTRODUCTION

This Student Handout is designed to help the experienced technician in troubleshooting the Model 6160. There are three sections to this Handout: BLOCK DIAGRAM ANALYSIS; FUNCTIONAL BLOCK DIAGRAM ANALYSIS; and TROUBLESHOOTING. When performing calibration or troubleshooting procedures on the 6160 the Instrument Manual must be used. This Handout supplements the Instrument Manual and the 6160 service seminar.

The 6160 is a Frequency Synthesizer which generates discrete frequencies from 1 MHz to 160 MHz in two ranges, 1 to 12 MHz and 10 to 160 MHz. The output voltage is adjustable from +3 dBm to +13 dBm into 50Ω with the front panel control or external dc voltage.

The synthesis technique used in the 6160 is an indirect method employing Voltage Controlled Oscillators (VCO) and Phase Detectors in phase locked loop arrangements, which are referenced to a frequency standard. This arrangement insures accurate and stable output frequencies with low spurious signals and very low phase noise.

BLOCK DIAGRAM ANALYSIS

A simplified block diagram of the 6160 is illustrated in Figure 1. As shown, the 6160 can be divided into the following basic blocks. Frequency Standard, Input Filter, Computer, Digit Generators and Output Divider, with the synthesis process occurring withing the Digit Generators Front Panel or Remote control BCD commands are processed by the Computer and applied to the Digit Generators. These BCD digit commands direct the Digit Generators to produce discrete frequencies corresponding to each frequency dial selected on the front panel. These frequencies are combined to provide a coherent output from 80 to 160 MHz. The 80 to 160 MHz signal is applied to the Output Divider. Under commands by the Computer, the Output Divider divides the input frequency by 1, 2, 4, 8, 10, 20, 40 or 80 to yield the frequency selected on the front panel frequency dials (or remote control). Stability and accuracy of the output signal is based on the Frequency Standard. The standard may come from an external 5 MHz source or from one of the internal crystal oscillator options. The 5 MHz signal from the Frequency Standard is applied to the Input Filter where it is buffered and processed to provide a TTL level square wave output. This TTL output is applied to the Digit Generators as a reference for producing discrete frequencies.

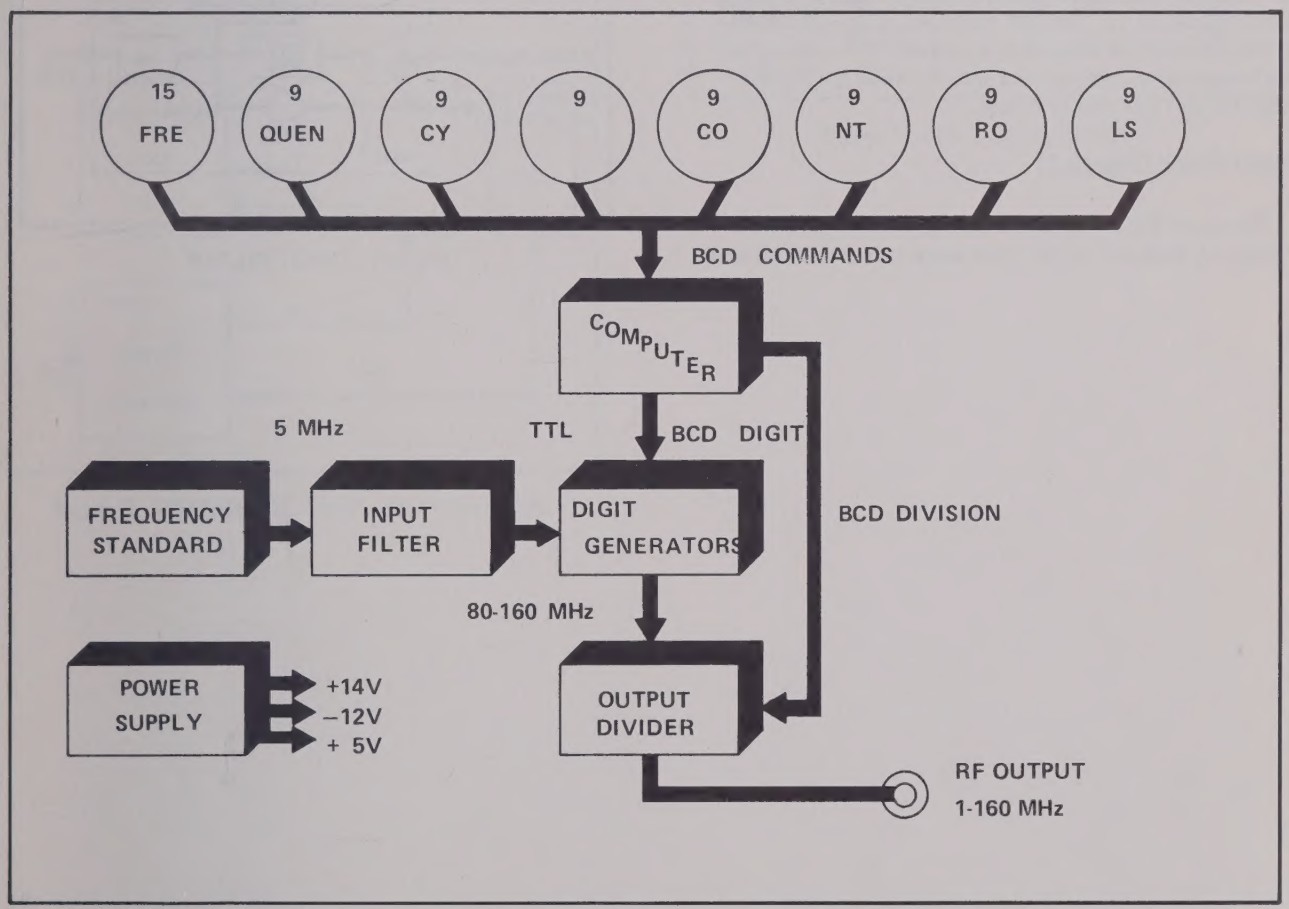


Figure 1. BLOCK DIAGRAM

FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

The following paragraphs describe operation of the synthesizer using the 6160 Function Block Diagram as found on page 7-5 of the manual. As you read through this analysis you will see functional Block Diagrams for each circuit analyzed.

Frequency Standard

The master oscillator for the frequency synthesizer can be either an external or internal 5 MHz standard. The internal standard is available in two options. One of these self-contained 5 MHz crystal oscillators is available as the –02 Option with 2 x 10^{-9} per day drift rate. The –02 option utilizes an oven for temperature control. The –05 option is a temperature compensated crystal oscillator (TCXO) with 5 x 10^{-6} per year drift rate.

Input Filter (Figure 2)

The Input Filter conditions and distributes the 5 MHz Frequency Standard signal. This signal is buffered, filtered, and amplified to provide two 5 MHz signals. It also incorporates a X2 multiplier to provide a 10 MHz signal. One of the 5 MHz signals is preset to a level of 1V rms into 50 ohms and made available at the BUFF 5 MHz OUT connector on the rear panel. The other 5 MHz signal is distributed to the 1 MHz Digit Unit Step Loop, for a reference. The 10 MHz signal is applied as a reference to the 10 MHz D.U. Step Loop Phase Detector.

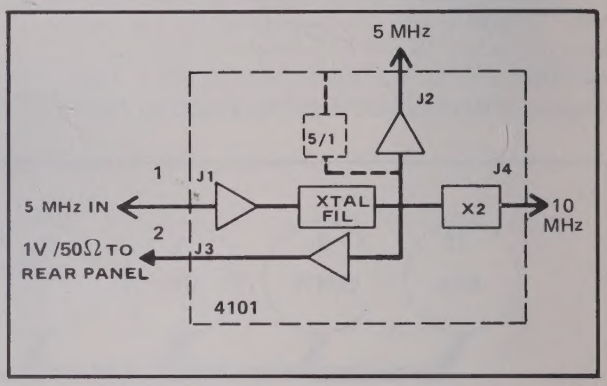


Figure 2. INPUT FILTER

Reference Frequency Distribution (Figure 3)

The 5 MHz signal to the 1 MHz Digit Unit Step Loop module is divided to 1 MHz by a 5/1 divider. This signal functions as a reference for the 1 MHz D. U. Step Loop. It is also applied to the Six Digit Generator where it is buffered and applied to the Computer as a clock signal. The 1 MHz reference undergoes further division for use by the Six Digit Generator.

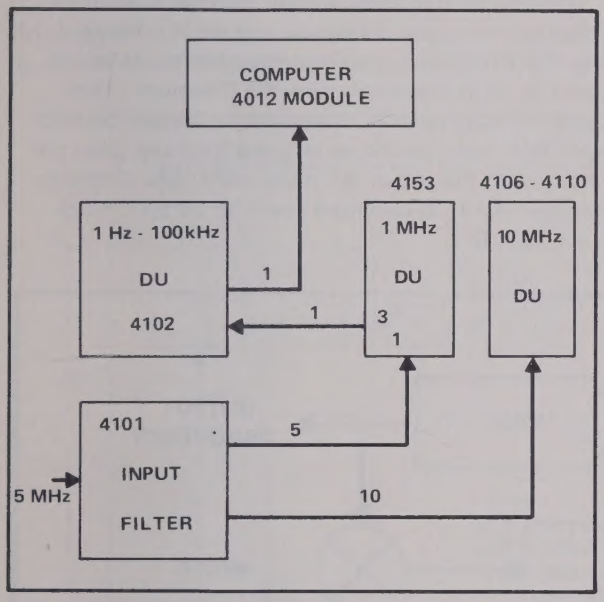


Figure 3. REFERENCE FREQ. DISTRIBUTION

Digit Generator (Figure 4 – 8)

Figure 4 illustrates the composition of the Digit Generators discussed in the Simplified Block Diagram description. Frequencies for the six lower order decades, 1 Hz through 100 kHz, are produced in the Six Digit Generators, respectively. The same basic circuit arrangement is used in each generator and will be described in the following paragraph.

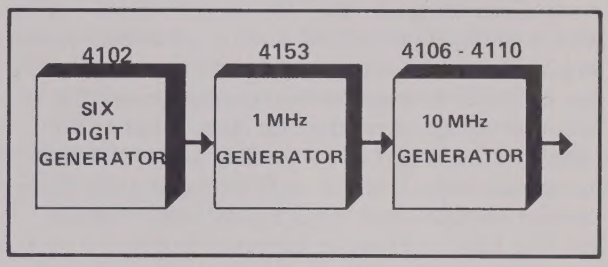


Figure 4. DIGIT GENERATORS

Figure 5 illustrates the basic phase lock loop circuit arrangement used for each decade in the generators. The arrangement consists of Main Loop and Step Loop circuitry. Frequency steps for each digit are produced in the Step Loop. These steps are then added to the preceeding decade frequency in the Main Loop circuit.

Beginning with the Step Loop, a reference frequency derived from the synthesizer's frequency standard is applied to one input of the phase detector. A divided down Step Loop VCO frequency is applied to the other input. Any difference between the two frequencies results in a dc control voltage output from the Phase Detector. This control voltage is applied to the Step Loop VCO and changes the output frequency until the inputs to the Phase Detector are equal, resulting in a phase lock condition. The Step Loop VCO output frequency is applied to one input of the Main Loop Mixer where it is mixed with the Main Loop VCO frequency. The Mixer output is applied to the Low Pass Filter which yields the difference frequency. A control voltage from the Main Loop Phase Detector changes the VCO frequency until the difference frequency equals the preceding decade frequency. This results in a Main Loop VCO output frequency which is equal to the Step Loop VCO frequency plus the preceding decade frequency.

Varying the frequency steps in a decade is accomplished by varying the division ratio of the N:1 Divider. The N:1 Divider is a programmable counter. It can be preset by BCD commands from the Computer. How much the Step Loop VCO frequency is divided depends upon how many counts are required from any given preset count to the end of the count cycle. The Computer programs the BCD command count by 2's up through the 1 MHz D. U.

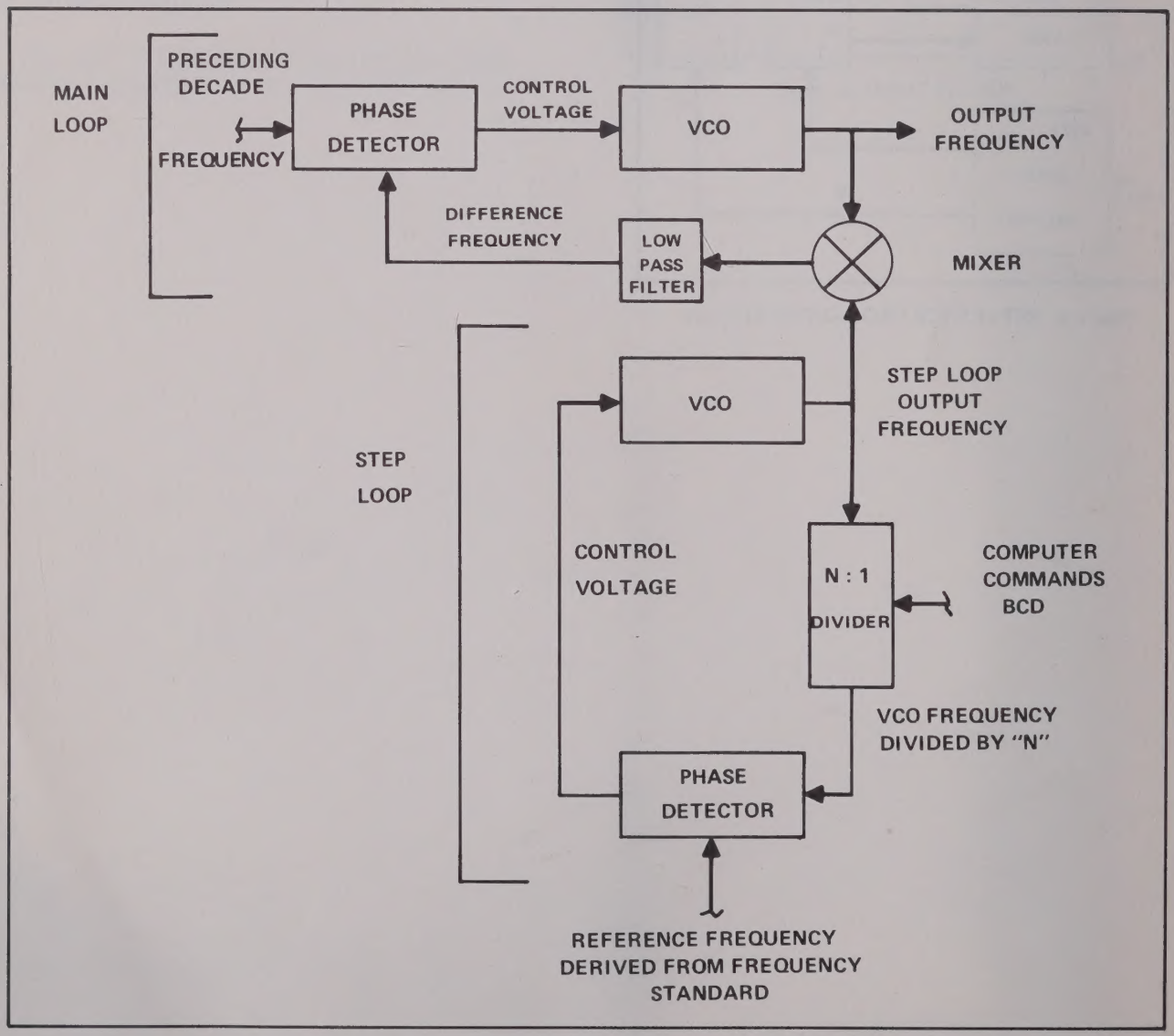


Figure 5. PHASE LOCK LOOP ARRANGEMENT

SIX DIGIT GENERATOR

Referring to Figure 6, the Six Digit Generator contains three loops that handle two decades of frequency control. The first loop, which is basically a step loop, controls the 1 Hz and 10 Hz decades. Here, the N:1 Divider has division ratios from 1100 to 1001. With zeros applied from the Computer to the 1 Hz and 10 Hz BCD control lines of the divider, a division ratio of 1100:1 is achieved. Consequently, with nines applied the ratio is 1001. To determine the frequency of the VCO, multiply the known division ratio by the reference frequency. For example, if zeros are applied, the ratio is 1100 which when multiplied by the 25 kHz reference equals 27.5 MHz.

In the 100 Hz and 1 kHz loop, the frequency steps are generated by a Step Loop and added to the preceding 1 Hz and 10 Hz frequency in the Main Loop. The N:1 Divider ratio is from 489, for zeros, to 390, for nines. The 10 kHz and 100 kHz circuit is similar in construction but with 2 N:1 Divider ratio of 205 to 304:1. This time with zeros programmed, the division is 205 : 1 and with nines programmed, 304: 1.

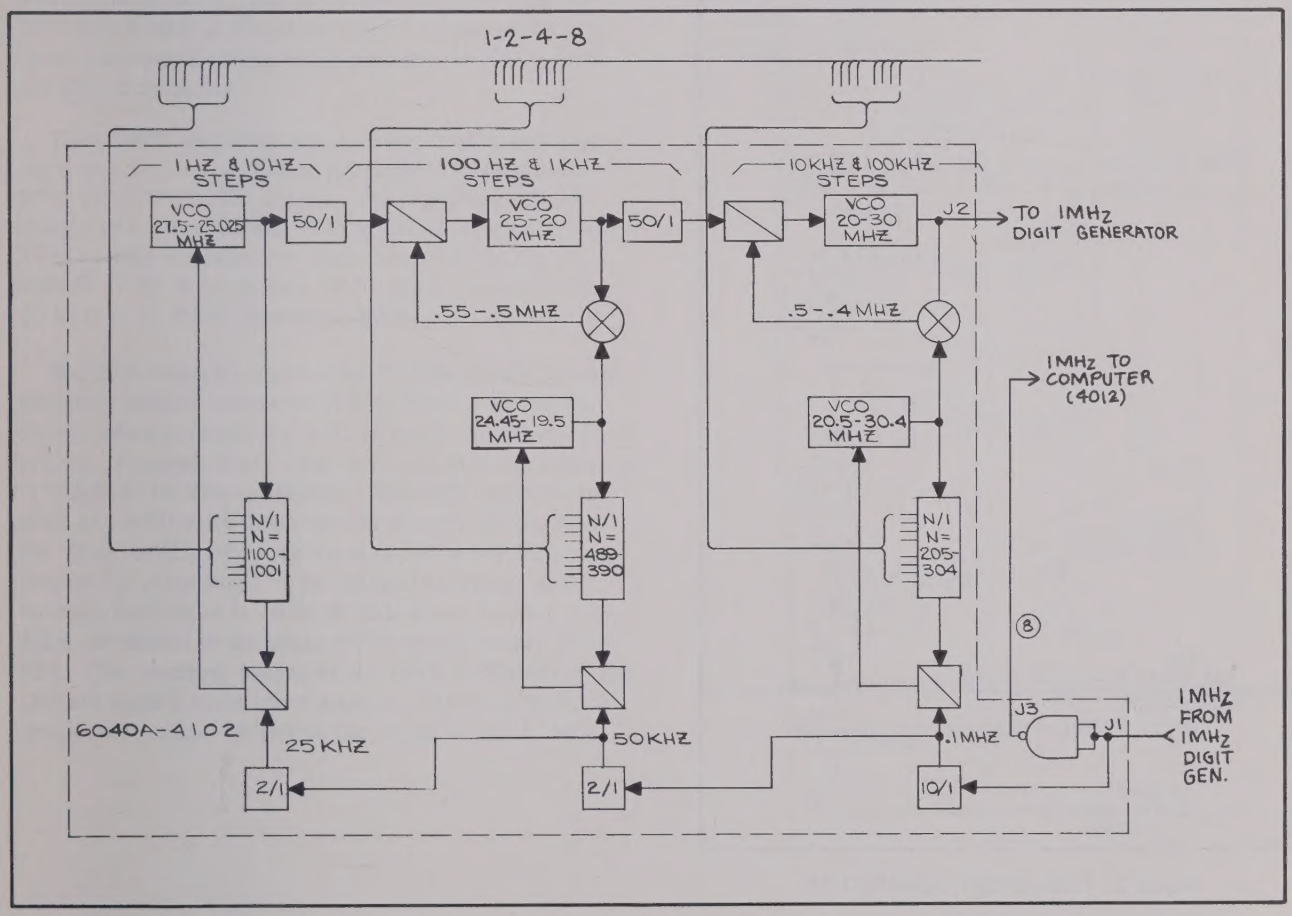


Figure 6. SIX DIGIT GENERATOR

1 MHz Digit Generator (Figure 7)

The 1 MHz Digit Generator must add its frequency steps to the preceding Six Digit Generator, therefore, it contains a Main Loop and Step Loop. Because the Main Loop VCO has a large frequency range, the loops are divided into three modules. These are the Step Loop, Main Loop VCO and the Main Loop Phase Detector. A 1 MHz reference frequency is used in the Step Loop which has a VCO range from 18-37 MHz. Consequently, the N : 1 Divider has division ratios of 18-37:1 in 20 steps. With the divider programmed for zero, the ratio is 18:1.

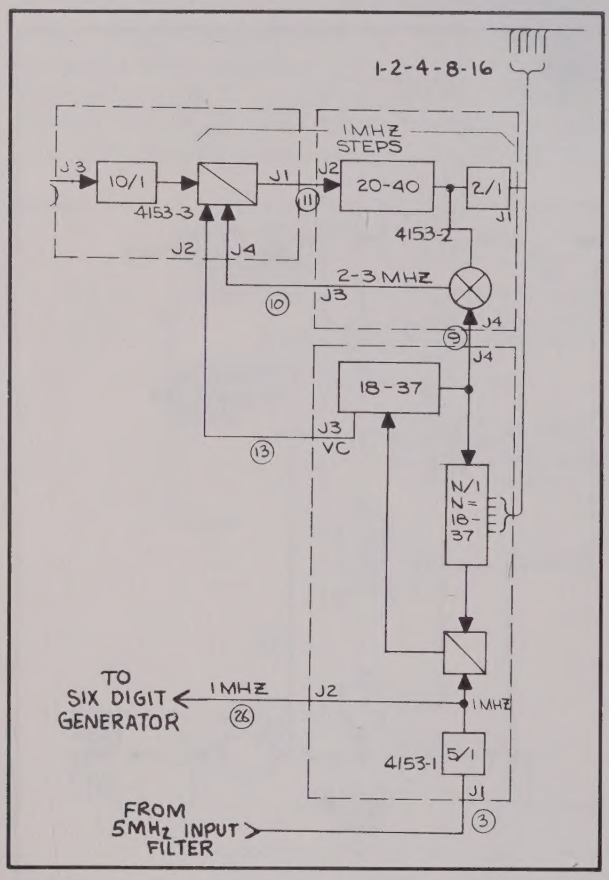


Figure 7. 1 MHz DIGIT GENERATOR

10 MHz Digit Section (Figure 8)

The 10 MHz Digit Section consists of five separate modules which together form the step and main loops shown in Figure 8. The output ranges from 80 to 159.999999 MHz. The step loop consists of modules titled 10 MHz Step Loop Phase Detector and 10 MHz, Step Loop VCO. The main loop consists of the 10 MHz IF Mixer, 10 MHz Phase Detector and 10 MHz Main VCO.

The 10 MHz step loop modules produce a 70 to 140 MHz output in 10 MHz increments. The circuitry associated with the 10 MHz step loop consists of a D/A converter, VCO, and a phase detector. The D/A converter receives the 10 MHz decade internal frequency control commands and produces a dc control voltage which presteers the VCO near to the desired frequency.

The 10 MHz main loop combines the 10 MHz step loop signal and the previous decade information to produce an 80 to 159.999999 MHz output. This signal is produced using a D/A converter and VCO in the 10 MHz D. U. Main VCO module, a subtractive mixture and LPF in the 10 MHz D. U. IF Mixer module, and a phase detector in the 10 MHz D. U. Phase Detector module.

The D/A converter receives the 10 MHz decade internal frequency control commands and produces a dc control voltage which presteers the VCO to nearly the desired frequency. Nominal overall range of the VCO is from 80 to 160 MHz in 10 MHz increments. The VCO output is applied to a subtractive mixer and the Output Divider Module. The 10 MHz step loop signal of 70 to 140 MHz functions as the other input to the subtractive mixer. Since the main loop signal is 10 to 20 MHz above the step loop signal, the output of the mixer will be approximately 10-20 MHz. The resulting output of the mixer is filtered in the LPF and applied to the phase detector. The phase detector compares the mixer output to the output of the 1 MHz Digit Unit Section and supplies a dc control voltage to the main loop VCO that phase locks the main loop such that both inputs to the phase detector are equal in frequency. The resulting 80 to 159.999999 MHz output from the VCO thus contains the entire digit information.

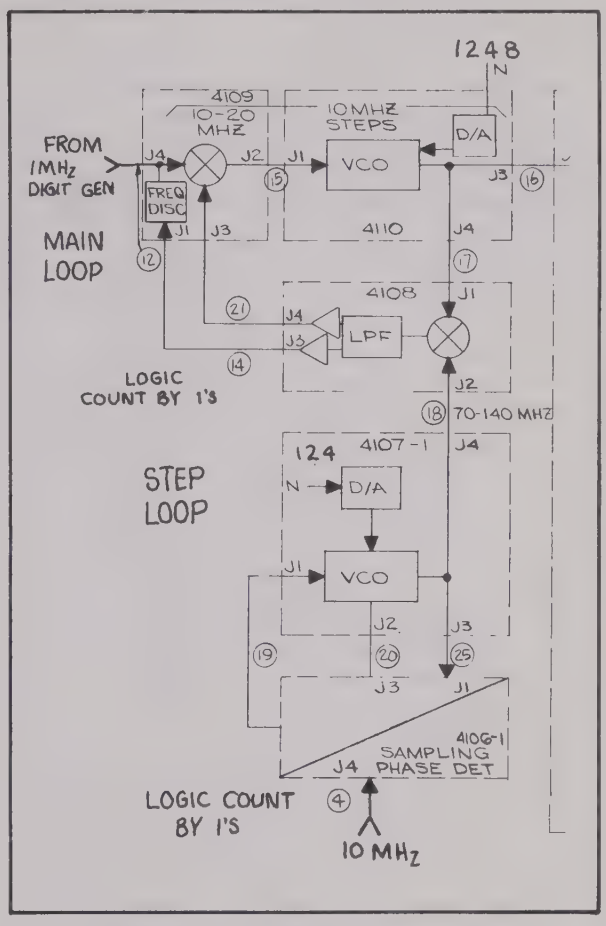


Figure 8. 10 MHz DIGIT GENERATOR

Output Divider (Figure 9)

The Output Divider receives the synthesized frequency of 80 to 159.999999 MHz and produces the final 1 MHz to 159.999999 MHz output. The circuitry consists of an input buffer, six 2/1 dividers, a 5/1 divider, low-pass filters, gates and an output amplifier.

The 80 to 159.999999 MHz signal is amplified in the input buffer and applied to a gate, low-pass filter, and a 2/1 divider. The 2/1 divider and each successive divider then provides dividend down signals to associated low-pass filters. Activation of the appropriate gate by the range and band commands from the frequency control computer then applies the desired low-pass filter output to the output amplifier.

This synthesized signal corresponds to the preselected output. For example, if a 13.111111 MHz output is selected, the 10 - 160 MHz range and 10 - 20 MHz band commands activates the gates for the 20 MHz low-Pass filter. Since the synthesized input to the Output Divider would be 104.888888 MHz, it is divided by three 2/1 dividers to obtain the preselected 13.111111 MHz output. The output amplifier then produces a +3 to +13 dBm output signal dependent upon the position of the OUTPUT LEVEL control or an external dc amplitude control voltage.

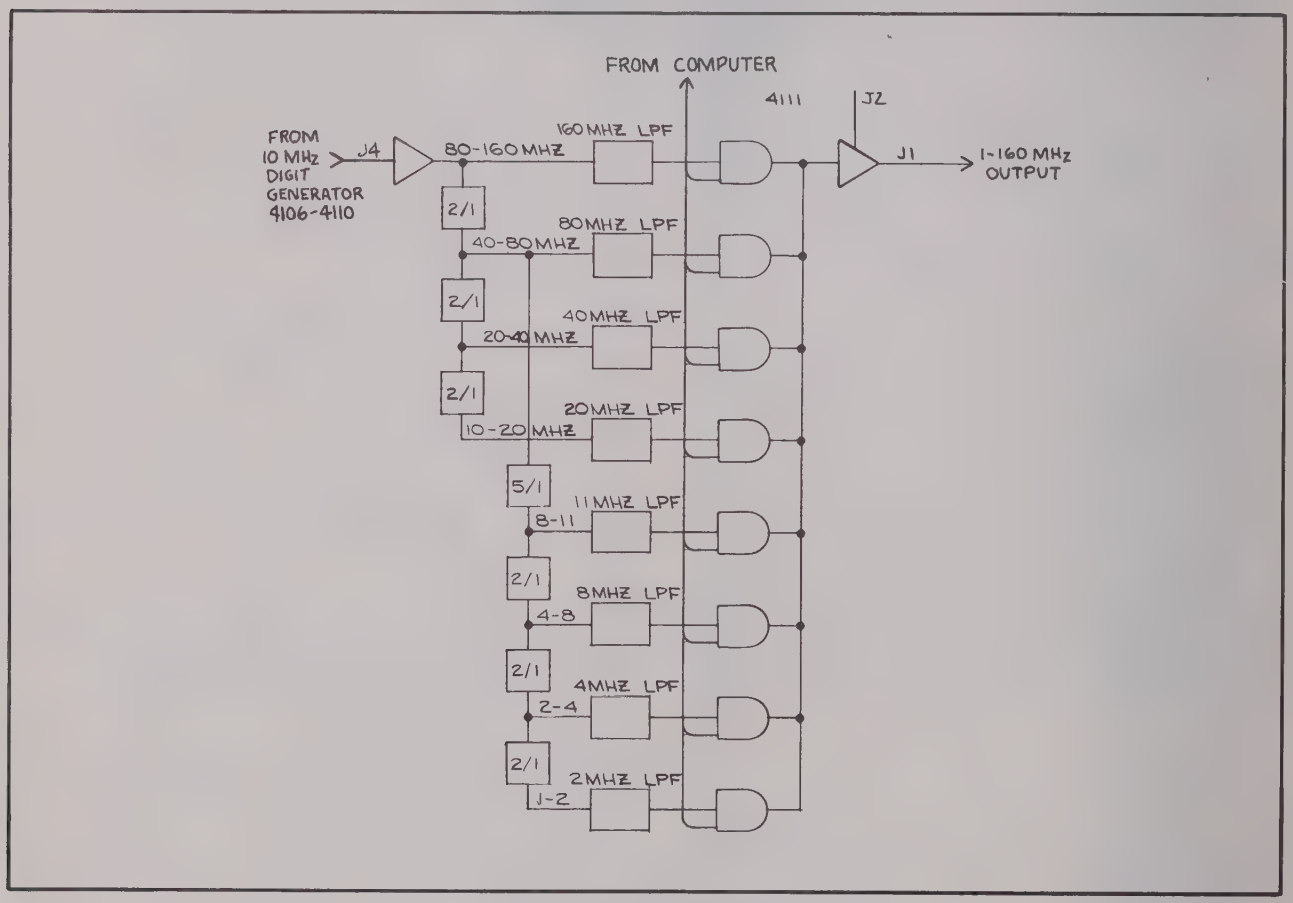


Figure 9. OUTPUT DIVIDER

Computer (Figure 10)

The frequency control Computer generates internal frequency control commands from manual or remote synthesizer frequency control inputs. Manual inputs are from the front panel frequency controls. Remote inputs are from the REMOTE FREQUENCY CONTROL connector on the rear panel. These inputs are multiplexed serial by decade, processed, and then converted to parallel digital commands that establish correct synthesis conditions necessary to obtain the preselected output. The following formula can be used to determine what digital output commands are generated for any preselected input.

INTERNAL FREQUENCY CONTROL COMMAND FOR 10 MHz = M x C_{IN}, FOR 1 MHz BELOW = 2 (M x C_{IN})

WHERE

C_{IN} = SYNTH. FREQ. CONTROL COMMAND

M = 1 for $C_{IN} \geq 80$ MHz
M = 2 for $40 \leq C_{IN} < 80$ MHz
M = 4 for $20 \leq C_{IN} < 40$ MHz
M = 8 for $10 \leq C_{IN} < 20$ MHz
M = 1 for $8 \leq C_{IN} < 12$ MHz
M = 2 for $4 \leq C_{IN} < 8$ MHz
M = 4 for $2 \leq C_{IN} < 4$ MHz
M = 8 for $1 \leq C_{IN} < 2$ MHz

Input commands from the front panel or rear panel are applied to the multiplexers. The band logic decodes the input information and selects the appropriate x1, x2, x4 or x8 gates. Range commands are applied with the band commands to the Output Divider to select dividers and gates in that module.

A 1 MHz clock input controls the parallel to conversion process. This input signal is applied to the load generator and divided by two to drive the address generator. The address generator produces binary address data to the multiplexer and address converter. The multiplexers serially transfer the parallel synthesizer frequency control BCD inputs in 1 Hz to 10 MHz decade order to the first x2 multiplier and the x1 gates. The output of the first x2 multiplier is applied to the following x2 multiplier as well as the x2 gates. The output of the second x2 multiplier is applied to the x4 gates as well as the final x2 multiplier, which produces the x8 output. Carry outputs are sequentially applied to the following multiplier by the carry "A" and "B" storage circuits. Carry load commands are derived from the load generator. The multiplied and gated serial by decade BCD information is then applied to the 1 MHz and 10 MHz storage circuits and x2 Multiplier. Conversion of the serial information to parallel format is done in the storage circuits. These circuits are addressed in sequence with each decade transfer period by control commands from the address converter.

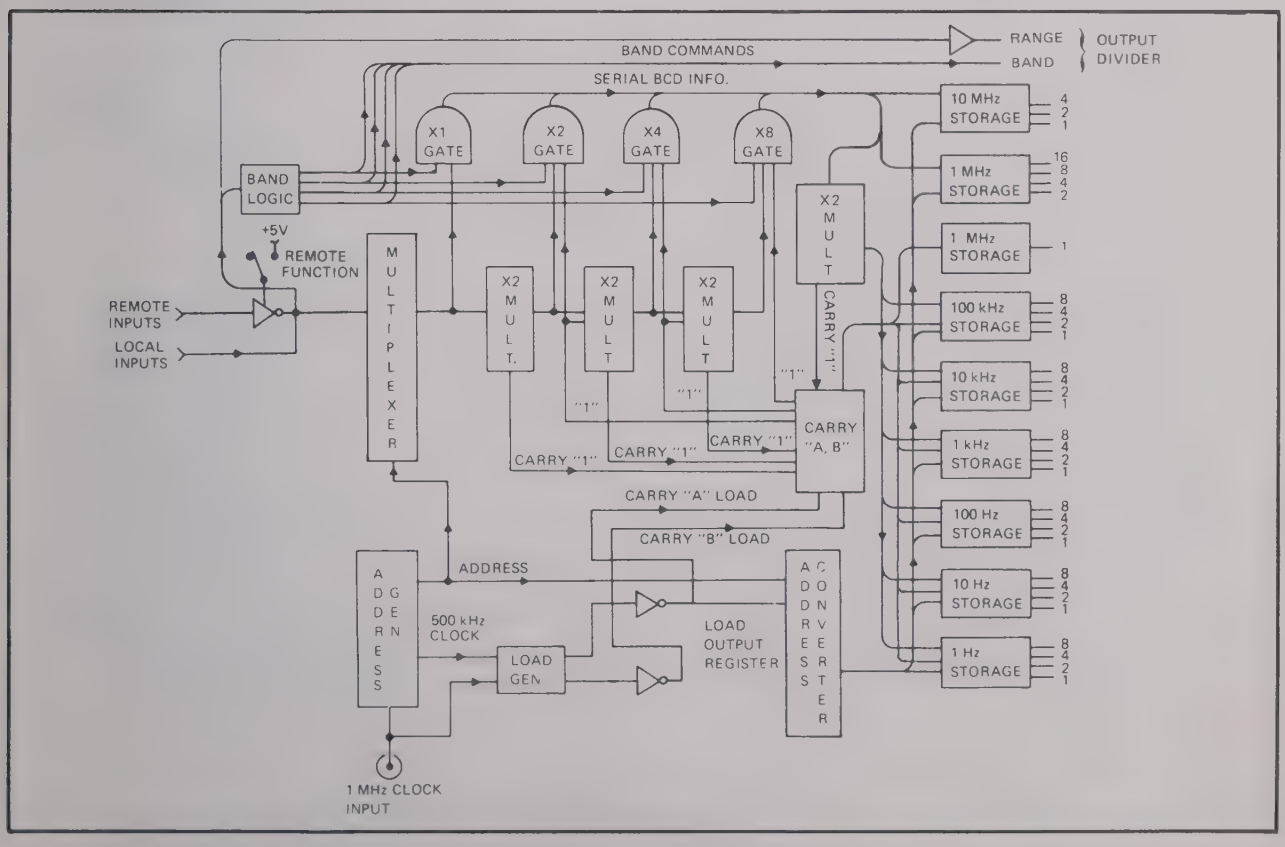


Figure 10. COMPUTER

TROUBLESHOOTING

To efficiently troubleshoot the 6160, a technician must first of all, know the theory of operation for the instrument. This theory can be found in block format in the handout, and in the instrument manual which explains the theory in schematic detail. Knowledge of the theory and use of the troubleshooting flow chart, also found in both the student handout and the instrument manual, will help in guiding the knowledgeable technician to the module level.

Listed below are some general notes of interest for use in troubleshooting the 6160.

GENERAL NOTES:

1. Proper Termination - Proper termination is achieved with a 50Ω load placed at the measuring instrument end of the coax.

2. Ground – Keep RF probes grounded sides connected to ground as close to the measuring point as possible.

3. Low Level Rf – Some low level RF signals may require the use of an oscilloscope input amplifier to give enough level into the frequency counter.

4. Start Point – For troubleshooting quickly, always start with 80 MHz dialed. This level requires no multiplication or division from the computer. Non-synthesis of any digit will indicate the level of the fault.

5. Spectrum Analyzer – A Spectrum Analyzer is a great troubleshooting tool for quick identification of a fault area when spurs or noise is suspected.

6. Service Kit – The service kit should be used to look at levels without interrupting the phase locked loops.

7. Substitution – Another synthesizer can be used to substitute modules from. Both synthesizers should be at the same frequency and locked to same standard source.

8. Counter – The Counter should always be locked to the same source as the synthesizer being checked.

9. Logic Level – +1 = High = True = +2.0 to +5.0V
0 = Low = False = 0.0 to +0.8V

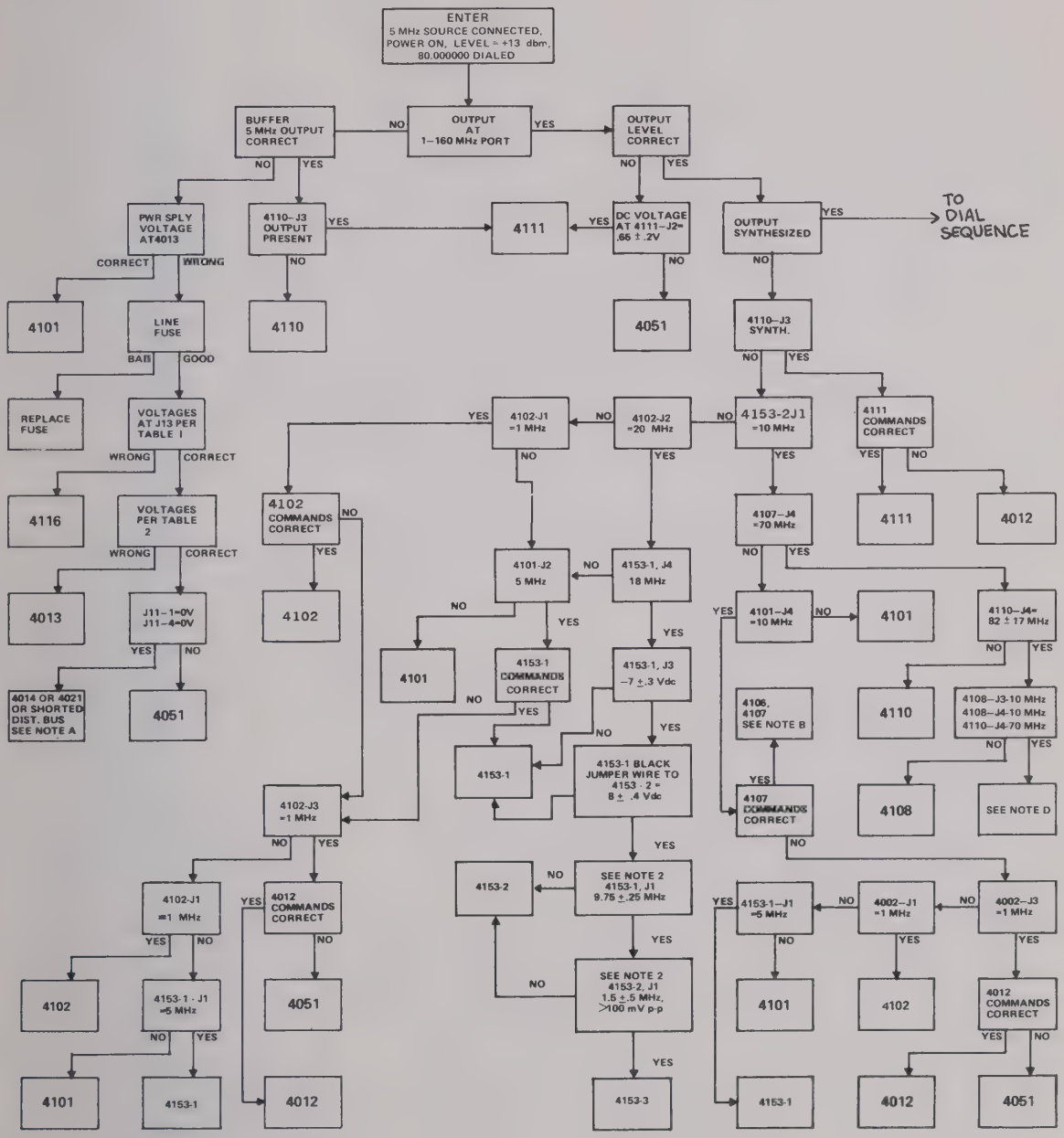
Equipment List for Troubleshooting to The Module Level.

TYPE	RECOMMENDED
Freq. Counter	Fluke 1952A/079
RF Voltmeter	HP 411 or equivalent
Digital Voltmeter	Fluke 8100 thru 8800
Scope	Tektronics 454 or equivalent
6160 Service Kit	Fluke # (6160A-7006) #339002

Miscl. Equipment:

a. 50Ω Terminations (2) min.
b. RF Cables - 50Ω R58A/μ etc. Minimum (4) (2 ft. to 4 ft. long)
c. Loax adapters of BNC type miscl. – TEE, (Male to female, etc.)
d. Hersh Clip Leads or equivalent for digital.
e. Aligator clip leads - 9 required (max.) (about 18 inches long)
f. Scope Probes X1 and X10.

To help you in proceeding to troubleshoot the 6160 a troubleshooting flow chart found on the next two pages has been inserted into this Handout. This is the same chart which appears in the Instrument Manual, and will help in giving direction and method of troubleshooting. Reference is made in the Troubleshooting Flow Chart, to Notes A, B, C, and D, and Tables 1 and 2. These notes and tables can be found immediately following the Flow Chart, and additional information is in the manual under Troubleshooting paragraphs, including module locations and interface data. It is a great aid to use the block diagram 1501 immediately following this Flow Chart in the manual.


ENTER
5 MHz SOURCE CONNECTED, POWER ON, LEVEL = +13 dbm, 80.000000 DIALED
BUFFER 5 MHz OUTPUT CORRECT
NO
OUTPUT AT 1–160 MHz PORT
YES
OUTPUT LEVEL CORRECT
NO
YES
NO
YES
PWR SPLY VOLTAGE AT4013
4110–J3 OUTPUT PRESENT
YES
4111
YES
DC VOLTAGE AT 4111–J2= .65 ± .2V
OUTPUT SYNTHESIZED
YES
TO DIAL SEQUENCE
CORRECT
WRONG
NO
NO
NO
4101
LINE FUSE
4110
4051
4110–J3 SYNTH.
BAD
GOOD
NO
YES
REPLACE FUSE
VOLTAGES AT J13 PER TABLE I
YES
4102-J1 =1 MHz
NO
4102-J2 =20 MHz
NO
4153-2J1 =10 MHz
4111 COMMANDS CORRECT
WRONG
CORRECT
YES
NO
4116
VOLTAGES PER TABLE 2
4102 COMMANDS CORRECT
NO
NO
YES
4107–J4 =70 MHz
4111
4012
WRONG
CORRECT
NO
YES
4013
J11–1=0V J11–4=0V
4102
4101-J2 5 MHz
NO
4153-1, J4 18 MHz
NO
YES
4101–J4 =10 MHz
NO
4101
4110–J4= 82 ± 17 MHz
YES
NO
YES
YES
YES
4101
4153-1 COMMANDS CORRECT
4153-1, J3 –7 ± .3 Vdc
4106, 4107 SEE NOTE B
4110
4108–J3-10 MHz 4108–J4-10 MHz 4110–J4-70 MHz
4014 OR 4021 OR SHORTED DIST. BUS SEE NOTE A
4051
NO
YES
NO
YES
NO
YES
NO
YES
4153-1
4153-1 BLACK JUMPER WIRE TO 4153 - 2 = 8 ± .4 Vdc
YES
4107 COMMANDS CORRECT
4108
SEE NOTE D
4102-J3 =1 MHz
NO
YES
NO
4153-2
SEE NOTE 2 4153-1, J1 9.75 ± .25 MHz
YES
4153-1–J1 =5 MHz
NO
4002–J1 =1 MHz
NO
4002–J3 =1 MHz
4102-J1 =1 MHz
4012 COMMANDS CORRECT
YES
NO
YES
NO
YES
NO
YES
NO
YES
4102
4153-1 - J1 =5 MHz
4051
SEE NOTE 2 4153-2, J1 1.5 ± .5 MHz, >100 mV p-p
4101
4102
4012 COMMANDS CORRECT
NO
YES
NO
YES
NO
YES
YES
4101
4153-1
4012
4153-3
4153-1
4012
4051

FLOWCHART

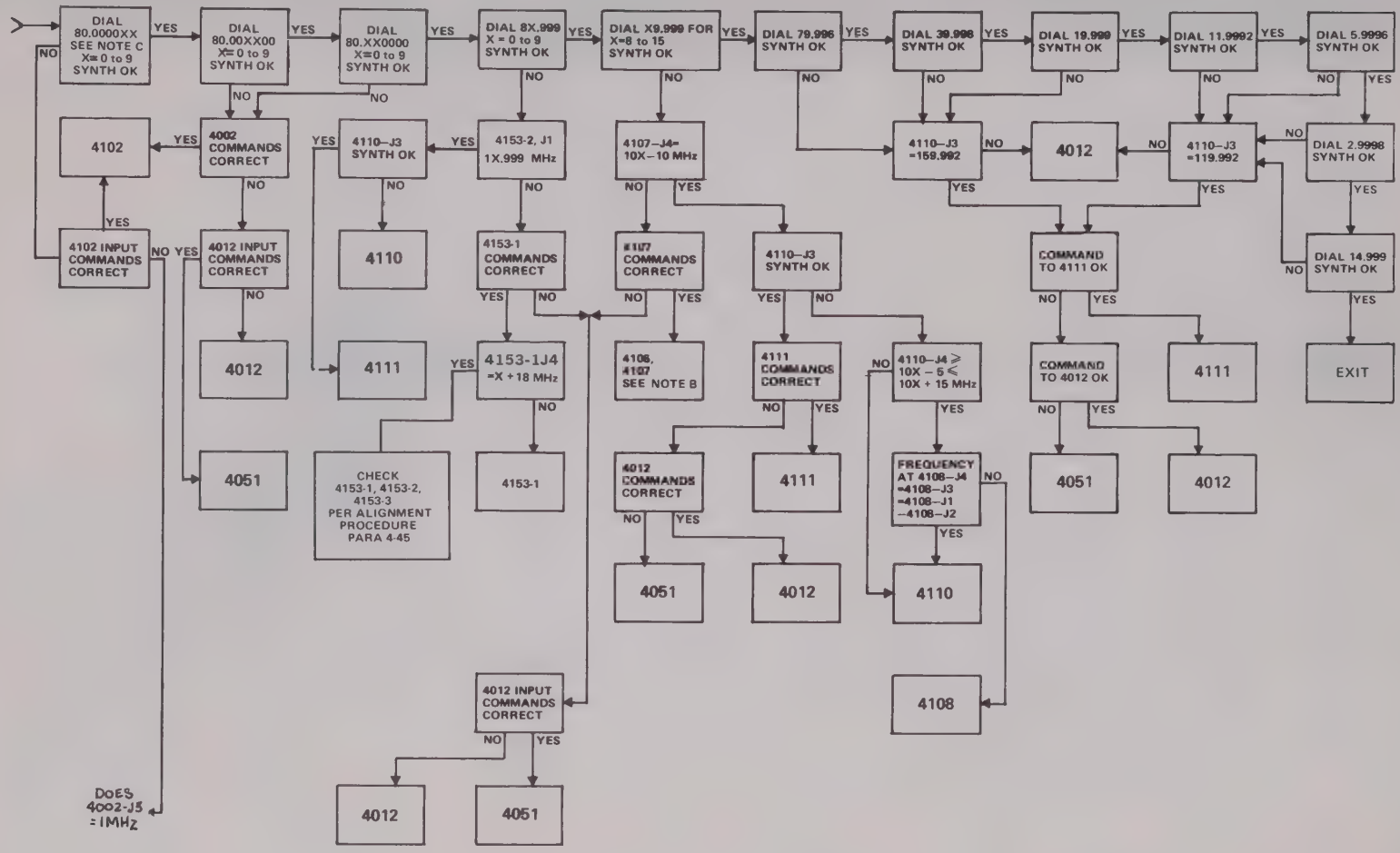

DIAL 80.0000XX SEE NOTE C X=0 to 9 SYNTH OK
DIAL 80.00XX00 X=0 to 9 SYNTH OK
DIAL 80.XX0000 X=0 to 9 SYNTH OK
DIAL 8X.999 X = 0 to 9 SYNTH OK
DIAL X9.999 FOR X=8 to 15 SYNTH OK
DIAL 79.996 SYNTH OK
DIAL 39.998 SYNTH OK
DIAL 19.999 SYNTH OK
DIAL 11.9992 SYNTH OK
DIAL 5.9996 SYNTH OK
DIAL 2.9998 SYNTH OK
DIAL 14.999 SYNTH OK
4102
4002 COMMANDS CORRECT
4110—J3 SYNTH OK
4153-2, J1 1X.999 MHz
4107—J4= 10X—10 MHz
4110—J3 =159.992
4012
4110—J3 =119.992
4102 INPUT COMMANDS CORRECT
4012 INPUT COMMANDS CORRECT
4110
4153-1 COMMANDS CORRECT
4107 COMMANDS CORRECT
4110—J3 SYNTH OK
COMMAND TO 4111 OK
4012
4111
4153-1J4 =X +18 MHz
4106, 4107 SEE NOTE B
4111 COMMANDS CORRECT
4110—J4 ≥ 10X — 5 ≤ 10X + 15 MHz
COMMAND TO 4012 OK
4111
EXIT
4051
CHECK 4153-1, 4153-2, 4153-3 PER ALIGNMENT PROCEDURE PARA 4-45
4153-1
4012 COMMANDS CORRECT
4111
FREQUENCY AT 4108—J4 =4108—J3 =4108—J1 =4108—J2
4051
4012
4051
4012
4110
4012 INPUT COMMANDS CORRECT
4108
DOES 4002-J5 = 1MHz
4012
4051
YES
NO

TABLE 1

PIN	AC VOLTAGE	PIN	AC VOLTAGE
1	0	A	(1) 0
2	0	B	0
3	19.7 ± 15%	C	19.7 ± 15%
4	0	D	0
5	0	E	0
6	19.7 ± 15%	F	19.7 ± 15%
7	9.9	H	9.9
8	9.9	J	9.9
9	9.9	K	9.9
10	9.9	L	9.9

NOTE: Gain access to J13 by removing top cover and hinging up 4102 module after removing the four screws securing it to synthesizer.

TABLE 2

TEST POINT	VDC
C3 (+) terminal	+25.2 ±15%
C2 (–) terminal	–25.4 ±15%
C1 (+) terminal	+11.7 ±15%

NOTE: Gain access to test points by removing top cover and hinging up the 4102 module after removing the four screws securing it to the synthesizer.

NOTE A

The –12V supply is used as a reference for the +14 and +5V supplies, therefore, a malfunction on the –12V supplies will make the +14V and +5V supplies inoperative.

NOTE B

Isolation of 4106-1 and 4107-1 problems. A signal at 4107-1J4 that is more than ±3 MHz from the desired frequency indicates a failure of the 4107-1 module. If the error is less than ±2 MHz the 4106-1 module is probably at fault. Remove connection to 4107-1J1 and check for the beat (error frequency) signal of 30 - 50 mV p-p into 50 ohm and less than 1.5 MVdc offset coming from the 4106-1 module. If no beat is present, there is a definite failure of the 4106-1 module. If beat is present, continue with the following two-step test.

a. Shunt 4107-1J1 with a 120 ohms resistor and remove connection to 4107-1J2. Load this port with a 1 kilohm load. Insert +40 μA into J1, (use a 0.35 megohm resistor to +14V supply). Check that frequency at 4107-1J4 is 1.7 to 3.3 MHz above desired frequency and that approximately minus 1.5 to –1.8V is across the 1 kilohm load at 4107-1J2.

b. With resistors installed as in step A., pull minus 40 Ma from 4107-1J1, (Use 0.3 megohm resistor to –12V supply). Check 4107-1J4 frequency. It must be 1.7 to 3.3 MHz below desired frequency and indicate from +1.0 to +1.2V across the load resistor on 4107-1J2. If condition described in steps A. and B. are not met, the 4107-1 Module is defective. If these conditions are met, the 4106-1 is faulty.

NOTE C

Vary the digit indicated by X and check for synthesis at each position of this switch in the case of all digits except the 10 MHz digit. For the 10 MHz digit range from 8 to 15.

NOTE D

Isolation of 4109 and 4110 troubles. Open connection to 4110-J1. Voltage at J1 must be less than ±0.4V. Apply 1.4 mA with a 10 kilohm resistor from the +14V supply into 4110. J1. Frequency at 4110-J3 must be higher than the 10 MHz dial setting by 15 MHz. Remove resistor to +14V supply and connect to –12V supply to draw 1.2 mA from 4110-J1. Frequency at 4110-J3 must be lower than 10 MHz dial setting by 5 MHz. If these conditions are not met the fault is in the 4110 module. If these conditions are met, the fault is likely in the 4109 Module.

NOTE 2

Connect J3 of 4153-1 to J2 of 4153-2.

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